Claims

What is claimed is:

1. A method for forming a semiconductor device capacitor, comprising:

providing a base dielectric layer;

etching said base dielectric layer to form an opening therein, said opening defined by first and second cross-sectional dielectric sidewalls;

forming a first conductive cross-sectional spacer on said first dielectric sidewall wherein said first conductive spacer forms a portion of a capacitor top plate;

forming a first capacitor cell dielectric layer on said first conductive spacer;

forming a second conductive cross-sectional spacer on said first capacitor cell dielectric layer;

forming a first conductive layer on said second conductive spacer, wherein said second conductive spacer and said conductive layer each form a portion of a capacitor bottom plate;

forming a second cell dielectric layer on said first conductive layer;

forming a second conductive layer on said second cell dielectric layer, wherein said second conductive layer forms a portion of said capacitor top plate; and

forming a conductive feature which electrically connects said first conductive spacer and said second conductive layer.

2. The method of claim 1, further comprising:

prior to etching said base dielectric layer, forming a third conductive layer over a planarized surface of said base dielectric layer;

during said etching of said base dielectric layer to form said opening, etching said third conductive layer to form an opening in said third conductive layer;

forming said first conductive cross-sectional spacer to contact said third conductive layer;

performing an etch which forms a cross-sectional third sidewall from said second conductive layer, said second cell dielectric layer, and said third conductive layer; and

during said formation of said conductive feature:

forming a conformal fourth conductive layer which contacts said second conductive layer and said third conductive layer;

spacer etching said forth conductive layer which forms a third conductive cross-sectional spacer on said third sidewall and electrically connects said first conductive spacer and said second conductive layer through said third conductive layer.

3. The method of claim 2 further comprising forming fourth and fifth conductive cross-sectional spacers from said fourth conductive layer within said opening in said base dielectric layer during said spacer etch of said fourth conductive layer.

4. The method of claim 2 further comprising removing at least a portion of said third conductive layer using a planarizing process prior to forming said second cell dielectric layer.

5. The method of claim 4 further comprising removing a portion of each of said first conductive cross-sectional spacer, said first capacitor cell dielectric layer, said second conductive cross-sectional spacer, and said first conductive layer during said planarizing process.

6. The method of claim 1 further comprising:

prior to etching said base dielectric layer, forming a third conductive layer over a planarized surface of said base dielectric layer;

during said etching of said base dielectric layer to form said opening, etching said third conductive layer to form an opening in said third conductive layer;

forming said first conductive cross-sectional spacer to contact said third conductive layer;

etching said second conductive layer and said second cell dielectric layer to form an opening therein and to expose said third conductive layer;

forming a conductive plug within said opening in said second conductive layer and said second cell dielectric layer, said plug contacting said second conductive layer and said third conductive layer to electrically connect said first conductive spacer and said second conductive layer through said third conductive layer.

7. The method of claim 6 further comprising removing at least a portion of said third conductive layer by a planarizing process prior to forming said second cell dielectric layer.

8. The method of claim 7 further comprising removing a portion of each of said first conductive cross-sectional spacer, said first capacitor cell dielectric layer, said second conductive cross-sectional spacer, and said first conductive layer during said planarizing process.

9. A method used to form a semiconductor device, comprising:

providing a semiconductor wafer substrate assembly comprising a semiconductor wafer and a conductive contact pad overlying said wafer;

forming an etch stop layer on said contact pad;

forming a blanket planarized base dielectric layer on said etch stop layer;

forming a conformal first conductive layer on said planarized base dielectric layer;

etching said conformal first conductive layer and said planarized base dielectric layer to form first and second cross sectional sidewalls in said base dielectric layer which define a recess in said base dielectric layer, wherein said etch exposes said etch stop layer;

forming a second conductive layer which comprises a first conductive spacer on said first sidewall;

forming a first cell dielectric layer on said first conductive spacer and on said etch stop layer;

forming a third conductive layer on said first cell dielectric layer;

spacer etching said third conductive layer and said first cell dielectric layer to form a second conductive spacer from said third conductive layer, to form a cell dielectric spacer from said first cell dielectric layer, and to expose said etch stop layer;

subsequent to said spacer etching said third conductive layer and said first cell dielectric layer, etching said etch stop layer to expose said contact pad;

forming a fourth conductive layer on said second conductive spacer and on said contact pad;

forming a second cell dielectric layer on said fourth conductive layer;

forming a fifth conductive layer on said second cell dielectric layer; and

electrically connecting said first conductive spacer and said fifth conductive layer, wherein said second and fifth conductive layers form a first capacitor plate, and said third and fourth conductive layers form a second capacitor plate interposed between said first conductive spacer and said fifth conductive layer.

10. The method of claim 9 further comprising:

during said formation of said second conductive layer, forming said spacer to contact said first conductive layer;

etching an opening in said second cell dielectric layer and said fifth conductive layer to expose said first conductive layer;

forming a conductive plug within said opening in said fifth conductive layer and said second cell dielectric layer, said plug contacting said first conductive layer and said fifth conductive layer to electrically connect said first conductive spacer and said fifth conductive layer through said first conductive layer.

11. The method of claim 9 further comprising:

performing an etch which forms a third cross-sectional sidewall from said fifth conductive layer, said second cell dielectric layer, and said first conductive layer;

forming a sixth conductive layer over said fifth conductive layer and on said third cross-sectional sidewall; and

spacer etching said sixth conductive layer to form a conductive spacer on said third cross-sectional sidewall which electrically connects said first conductive spacer and said fifth conductive layer.

12. The method of claim 11 further comprising, during said formation of said sixth conductive layer, forming a portion of said sixth conductive layer within said opening in said base dielectric layer, wherein subsequent to spacer etching said sixth conductive layer, a portion of said sixth conductive layer remains in said opening in said base dielectric layer.

13. A semiconductor device comprising a plurality of container capacitors, with each container capacitor comprising, in cross section:

a first conductive layer which forms a first conductive spacer;

a first cell dielectric layer which forms a cell dielectric spacer and which contacts said first conductive spacer;

a second conductive layer which forms a second conductive spacer, which contacts said first said first cell dielectric spacer, and which is electrically isolated from said first conductive spacer;

a third conductive layer which contacts said second conductive layer;

a second cell dielectric layer which contacts said third conductive layer;

a fourth conductive layer which contacts said second cell dielectric layer;

a fifth conductive layer contacts said first conductive layer; and

a conductive feature which contacts said fourth conductive layer and said fifth conductive layer and electrically connects said first conductive layer with said fourth conductive layer,

wherein said first conductive layer and said fourth conductive layer provide at least a portion of a capacitor top plate and said second conductive layer and third conductive layer provide at least a portion of a capacitor bottom plate.

14. A container capacitor for a semiconductor device comprising:

a first capacitor top plate layer having a generally cylindrical shape comprising an internal surface and an external surface;

a first cell dielectric layer having a generally cylindrical shape comprising an internal surface and an external surface, wherein said external surface of said first cell dielectric layer contacts said internal surface of said first capacitor top plate layer;

a first capacitor bottom plate layer having a generally cylindrical shape comprising an internal surface and an external surface, wherein said external surface of said first capacitor bottom plate layer contacts said internal surface of said first cell dielectric layer;

a second capacitor bottom plate layer having a generally cylindrical shape comprising an internal surface and an external surface, wherein said external surface of said second capacitor bottom plate layer contacts said internal surface of said first capacitor bottom plate layer;

a second cell dielectric layer having a generally cylindrical shape comprising an internal surface and an external surface, wherein said external surface of said second cell dielectric layer contacts said internal surface of said second capacitor bottom plate layer; and

a second capacitor top plate layer having a generally cylindrical shape comprising an internal surface and an external surface, wherein said external surface of said second capacitor top plate layer contacts said internal surface of said second cell dielectric layer.

15. The container capacitor of claim 14, further comprising a conductive contact pad which contacts said second capacitor bottom plate layer and does not contact said first capacitor bottom plate layer but is electrically coupled to said first capacitor bottom plate layer through said second capacitor bottom plate layer.

16. The container capacitor of claim 14, further comprising:

a base dielectric layer having an horizontal upper first surface and a vertically-oriented second surface which defines a generally cylindrical shape, wherein said external surface of first capacitor top plate layer contacts said second surface of said dielectric layer; and

a conductive layer on said horizontal upper surface of said base dielectric layer, wherein said first capacitor top plate layer is electrically coupled to said second capacitor top plate layer through said conductive layer.

17. The container capacitor of claim 16, further comprising a conductive spacer which contacts both said second capacitor top plate layer and said conductive layer on said horizontal upper surface of said base dielectric layer, wherein said first capacitor top plate layer is electrically coupled to said second capacitor top plate layer through said conductive spacer.

18. The container capacitor of claim 17 wherein said conductive spacer is a first conductive spacer and said container capacitor further comprises at least a second conductive spacer which contacts said internal surface of said second capacitor top plate.

19. The container capacitor of claim 16, further comprising a conductive plug which contacts both said second capacitor top plate layer and said conductive layer on said horizontal upper surface of said base dielectric layer, wherein said first capacitor top plate layer is electrically coupled to said second capacitor top plate layer through said conductive plug.